Silicon Nitride on Silicon-on-Insulator: a Platform for Integration Active Control over Passive Components

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Abstract: We propose the use of SOI with silicon nitride layers for electronic control. A phase modulator with a $V_\pi \cdot L$ of 1.02 V·mm and a compact vertical coupling taper are demonstrated in an easy-to-fabricate planar structure.
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1. Introduction

In recent years, silicon nitride (SiN) on silicon-on-insulator (SOI) platforms have drawn tremendous interest as a promising solution to integrated optical interconnections. SiN-on-SOI platforms enable the combination of the passive optical functionalities implemented in the SiN layer with the active functionalities in the SOI. Compared to silicon (Si), the lack of two photon absorption and free carrier absorption, along with the small nonlinear susceptibility $\chi^{(3)}$ renders SiN more suitable for high power applications. Its low thermal-optic coefficient makes SiN devices more robust against temperature variations. In addition, the moderate refractive index contrast of SiN and silica reduces the SiN waveguides' vulnerability to sidewall roughness scattering. Attracted by these advantages, several optical components, e.g. antennas [1], arrayed waveguide gratings [2], and polarization rotator-splitters [3], have been demonstrated on the SiN-on-SOI platforms. However, most efforts are devoted to tapers [4] or grating couplers [5], designed to completely transfer power from one layer to another and then perform functionalities on individual layers. Thus, there is a gap in employing several layers simultaneously to achieve full integration.

Here, we present the design of a phase modulator utilizing SiN/SiO_2/Si layers. The Si layer is doped to be a *p-i-n* diode that operates in carrier-injection-mode. A SiN stripe is stacked on the Si intrinsic region to laterally confine the electromagnetic waves. The modulator has a half-wave voltage-length product ($V_\pi \cdot L$) of 1.02 V·mm, and a chirp factor (CF) of 18.42. A Si taper with a coupling coefficient of -0.14 dB and a coupling length L_c of 20 μm is designed to transfer power from the modulator to the SiN waveguide. The merit of the design is the simple structure which is in favor of fabrication, and the highly efficient short taper made possible by the mode distribution in both the SiN and Si layers.

2. Modulator Design

The cross section of the modulator structure in the *x-y* plane is shown in Fig. 1(a). The modulator is built on an SOI substrate with the device layer thickness denoted as H_{Si}. A 20 nm thick SiO_2 layer (H_{gap} = 20 nm) is deposited for the ease of SiN fabrication. The height of the SiN layer is set to be 300 nm (H_{wg} = 300 nm) to avoid stress-induced film cracking. The Si slab is doped symmetrically with an intrinsic region (*p*-type, 10^{15} cm^{-3}) as wide as the SiN stripe W_{wg}. The *n*+ and *p*+ regions are doped to be 10^{18} cm^{-3}, and they have the same width of $W_{n+} = W_{p+} = 2$ μm. The *n*++ and *p*++ regions are heavily doped to 5×10^{20} cm^{-3} in order to form good ohmic contact with the electrodes.

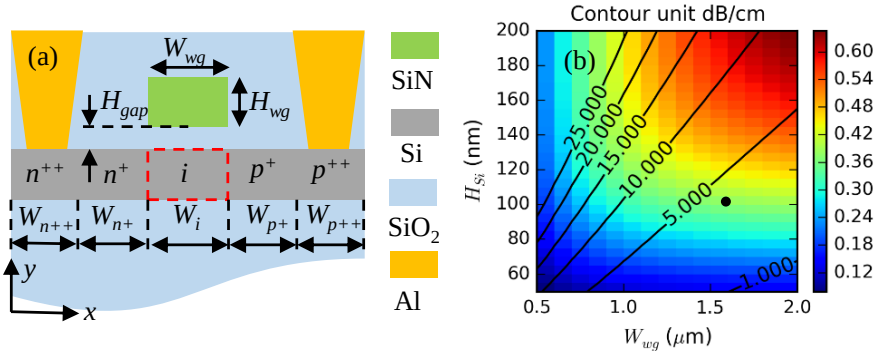

Fig. 1 (a) the modulator structure in the *x-y* plane. The intrinsic region is indicated by the red dashed rectangular. (b) The color map represents Γ_{Si}, and contour map reflects α as a function of the waveguide width W_{wg} and the Si slab thickness H_{Si}. The black dot represents the geometry that is adopted in our design.

The strip load waveguide supports the fundamental TE (electric field along *x* axis) mode at 1550 nm wavelength. While the guided mode has its power distribution in both SiN and Si regions, we would like to maximize the power confined in the Si region to increase the modulation efficiency. To quantify the confinement, a parameter Γ_{Si} is defined by taking the ratio of the power inside the intrinsic region (red dashed rectangle in Fig. 1(a)) to the total

power. However, increasing Γ_{Si} will in turn lead to a higher propagation loss α due to the doped Si absorption. As a tradeoff between Γ_{Si} and α, the waveguide is optimized to be (W_{wg}, H_{Si}) = (1.6 μm, 100 nm) as indicated by the black dot in Fig. 1(b). The color map shows Γ_{Si} and the contour shows α as a function of W_{wg} and H_{Si}.

Electronic simulation finds the *p-i-n* threshold voltage to be ~0.7 V, above which significant mode refractive index and absorption coefficient changes are observed in Fig. 2(a). The 1 mm long phase modulator has a half-wave voltage-length product of 1.02 V·mm. At 1 V bias voltage, the CF, defined as $\delta n_{eff}/\delta\kappa_{eff}$ [6], is 18.42. The step response of the average free carrier density in the intrinsic region to a 1.1 V bias voltage is illustrated in Fig. 2(b). The rise time of ΔN_e is estimated to be 10 ns, indicating that the device can operate at speeds up to 50 MHz.

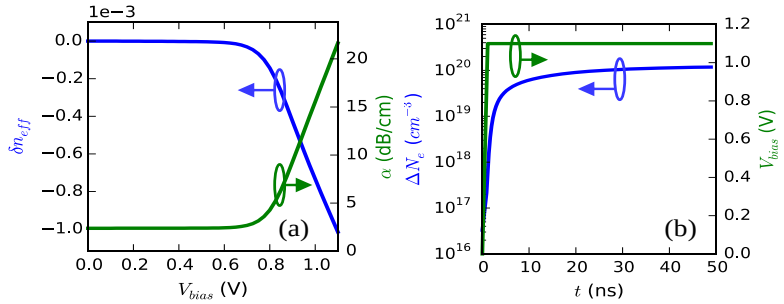

Fig. 2 (a) the refractive index change (left *y*-axis) and the absorption coefficient change (right *y*-axis) as a function of bias voltage V_{bias} in DC simulations. (b) The injected free carrier density (left *y*-axis) variation driven by a step bias voltage (right *y*-axis) in transient simulations. ΔN_e = ΔN_p, therefore, only ΔN_e is plotted.

3. Interlayer Transition

An adiabatic taper is used to transfer power from the modulator to the SiN waveguide and vice versa. The taper geometry is shown in Fig. 3(a) with the Si layer width shrunk from 3 μm to 100 nm. The coupling length L_c is 20 μm in our case. While most tapers suffer scattering loss from the tips at the end of the tapers, our design yields a remarkable coupling coefficient that is as large as -0.14 dB. The coupling coefficient can be even further improved to < -0.01 dB if L_c exceeds 50 μm. Thanks to the mode overlap in both Si and SiN regions, L_c can be designed even shorter to completely switch power from the modulator to the SiN waveguides.

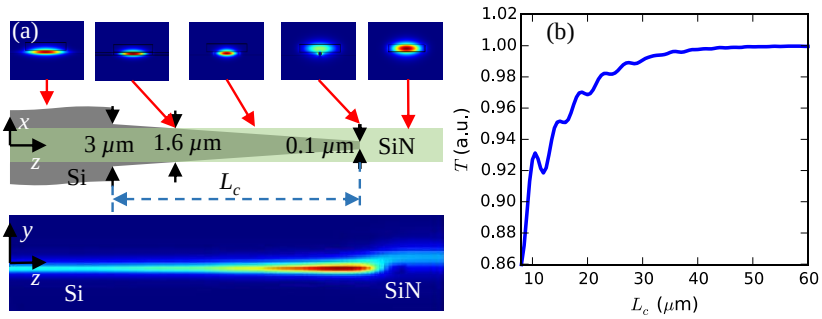

Fig. 3 (a) middle row, the taper geometry in the *x-z* plane. Upper row, the mode transition at different locations in the *x-y* plane. Bottom row, the power distribution in the *y-z* plane. (b) The coupling coefficient *T* as a function of the coupling length L_c.

4. Conclusion

We have demonstrated a SiN-stripe-loaded Si phase modulator on the SiN on SOI platform. Unlike previous devices, the modulator utilizes both SiN and Si layers for waveguiding with partial power in SiN waveguides, which facilitates a short taper design. In addition, it can also be used in high power applications because Si only interacts with a fraction of light. The advantage of the SiN-on-SOI platform is its simple structure that can used for fast prototyping. Optimizations to improve the modulation efficiency and speed, and investigations of its high power handling capability are currently underway.

1. Q. Zhao, et.al, "Experimental demonstration of directive Si3N4 optical leaky wave antennas with semiconductor perturbations at near infrared frequencies," in *Proc. SPIE 9365, Integrated Optics: Devices, Materials, and Technologies XIX* (International Society for Optics and Photonics, 2015), Vol. 9365, p. 93651K–93651K–10.
2. L. Chen, et.al, "Monolithically Integrated 40-Wavelength Demultiplexer and Photodetector Array on Silicon," IEEE Photonics Technol. Lett. **23**, 869–871 (2011).
3. W. D. Sacher, et.al, "Polarization rotator-splitters and controllers in a Si_3N_4-on-SOI integrated photonics platform," Opt. Express **22**, 11167 (2014).
4. W. D. Sacher, et.al, "Multilayer Silicon Nitride-on-Silicon Integrated Photonic Platforms and Devices," J. Light. Technol. **33**, 901–910 (2015).
5. M. Sodagar, et.al, "High-efficiency and wideband interlayer grating couplers in multilayer Si/SiO_2/SiN platform for 3D integration of optical functionalities," Opt. Express **22**, 16767 (2014).
6. A. Vonsovici and A. Koster, "Numerical simulation of a silicon-on-insulator waveguide structure for phase modulation at 1.3 mu;m," J. Light. Technol. **17**, 129–135 (1999).